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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/620,469 | 07/15/2003 | Timothy S. Beatty | 42P15523 | 8633 |

8791 7590 12/10/2004

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| EXAMINER | |
|---|---|
| NGUYEN, DANG T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2824 | |

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/620,469 | BEATTY ET AL. | |
| | Examiner | Art Unit | |
| | Dang T Nguyen | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 – 12, and 16 – 19* is/are pending in the application.

4a) Of the above claim(s) *13-15 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1, 2, 6 – 8, 11, and 16 – 19* is/are rejected.

7)☐ Claim(s) *3 – 5, 9, 10 and 12* is/are objected to.

8)☐ Claim(s) *1-20* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

## DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on July 15, 2003.

2. Claims 1 – 20 are pending in this case. Claims 1, 13, and 16 are independent claims.

### *Election/Restrictions*

3. Applicant's election without traverse of claims 1 – 12, and 16 – 19, in the reply filed on 10/26/04 is acknowledged. Claims 13 – 15 and 20 are canceled.

### *Claim Objections*

4. Claim 18 objected to because of the following informalities: " according to claim 18". Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 1, 2, 6 – 8, 11, and 16 – 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi U.S. patent No. 6,175,532 B1 – filed: May 21, 1999.**

**Regarding independent claim 1**, Fig. 64 ([1602]) of Ooishi disclose memory driver (Fig. 54) comprising: selection logic (Fig. 6 [1610]), to receive an address (Fig. 6

[Input Address]) for promotion to a memory (Fig. 54 [1600]) and to provide an indication (Fig. 64 [Coincidence/Non-coincide]) of whether to promote the received address ([1614] or a modified version [1612]) thereof to the memory (Fig. 54 [1600]); and a multiplexing element (Fig. 64 [1616]), responsive to the selection logic (Fig. 64 [Coincidence/non-coincidence]), to selectively promote either the received address (Fig. 64 [1614]) or the modified version (Fig. 64 [1614]) thereof to the memory based, at least in part, on the received indication (Fig. 64 [Coincidence/non-Coincidence]).

**Regarding dependent claim 2**, Fig. 30 of Ooishi further discloses a memory driver according a latch element (Fig. 30 [To ADDRESS LATCH of each ARRAY Block]), coupled to the multiplexing (Fig. 3 [206]) element, to assert address content received from the multiplexing element to the memory (Fig. 54 [1600]).

**Regarding dependent claim 6**, Ooishi discloses the selection logic (Fig. 64 [1610]) comprising detection logic (Col. 65 lines 37 – 42 disclosing the selection logic 1610 is detecting by comparing), to determine whether at least a subset of received address is composed of zeroes (Col. 58 lines 32 - 33).

**Regarding dependent claim 7**, Ooishi discloses wherein the detection logic is a one-detect circuit (Col. 58 lines 33 – 35).

**Regarding dependent claim 8**, Ooishi discloses the selection logic (Fig. 64 [1610]) comprising: detection logic (Col. 65 lines 37 - 42 disclosing the selection logic 1610 is detecting by comparing), to determine whether at least a subset of the received address is composed of a predefined value (Col. 65 lines 25 – 31 and 37 – 42).

**Regarding dependent claim 11**, Fig. 44 of Ooishi further discloses the latch comprising: a first and second differential set of transistors (458, 460) , coupled to the multiplexing element, to assert either the received address (BS.SN) and complement thereof, or the PID and complement thereof to a memory device (470, 475).

**Regarding independent claim 16**, Fig. 64 [1602] of Ooishi discloses method implemented within a memory driver (Fig. 54[1602]) comprising: receiving at least a subset (Fig. 64 [A1 – A8]) of an address for promotion to a memory (Fig. 54 [1600]); and selectively replacing (Fig. 64 [1616]) at least the subset of the received address with a process identifier (Fig. 64 [1612]) if it is determined that the subset of the received addresses is composed of zeroes (Col. 58 lines 45 – 50).

**Regarding dependent claim 17**, Fig. 55C of Ooishi further comprising: analyzing the received subset (A3, A4) of the address (A1, A2, A3, A4) to determine whether the subset of composed of zeroes (first row of A3, A4 in Fig. 55C) and, if so, to provide an indication (Fig. 64 [Coincide]) to a multiplexing element (Fig. 64 [1616]) to replace the received subset of the address with the process identifier (Fig. 64 [1616]).

**Regarding dependent claim 18**, Ooishi discloses a method implemented within a memory driver (Fig. 64) according to claim 18, further comprising: asserting either the received address [1614], or a modified version [1612] thereof based, at least in part, on whether the received subset of the address is composed of zeroes (Col. 58 lines 32 – 34).

**Regarding dependent claim 19**, Fig. 1 of Ooishi discloses a storage medium comprising content which, when executed by an accessing machine, causes the machine to generate a memory driver according to claim 16 (Col. 6 lines 35 – 44).

***Allowable Subject Matter***

4. Claims 3 – 5, 9, 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**With respect to claim 3**, in addition to other elements in the respective claim, the prior art fails to teach or suggest "the latch element comprising: a pulse generator element, to receive a clock signal and produce at least two reference signals, overlapping yet offset from one another in time; and one or more driver elements, coupled to the multiplexing element and responsive to the pulse generator element, to receive content promoted from the multiplexing element during a precharge phase the reference signals, and to assert the content received from the multiplexer to the memory during a discharge phase of the reference signals".

**With respect to claim 9**, in addition to other elements in the respective claim, the prior art fails to teach or suggest "the selection logic comprising: a first and second set of stacked transistors, wherein individual transistors of the first set are coupled to receive at their gate one of an indication from the selection logic, an address, and a process identification value, while individual transistors of the second set are coupled to receive at their gate a complement of the indication, the address and the Pm value".

**With respect to claim 12**, in addition to other elements in the respective claim, the prior art fails to teach or suggest "wherein the latch is coupled to the multiplexing element through a transistor responsive to a pulse generator, such that the latch is isolated from the multiplexing element during a precharge phase of the pulse generator, and asserts content at the output of the multiplexing element during a discharge phase of the pulse generator".

### *Prior art*

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

| | | |
|---|---|---|
| Pon | Patent No.: 5,805,517 | Date of Patent: Sep. 8, 1998 |
| Choi et al. | Patent No.: US 6,317,351 | Date of patent: Nov. 13, 2001 |
| Akaogi et al. | Patent No.: US 6,201,753 B1 | Date of Patent: Mar. 13, 2001 |

### *Contact Information*

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703)

305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 12/3/2004

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER